

**Remarks**

Entry of the amendments, reconsideration of the application as amended, and allowance of all pending claims are respectfully requested. Claim 9 is canceled herein without prejudice, and new claims 15-17 are added. Claims 1-8 and 10-17 are now pending.

In the Office Action dated October 22, 2003, the title of the invention was objected to as not clearly indicative of the invention to which the claims are directed. Applicants acknowledge the suggested title but prefer the new title presented in the Amendments to the Specification. Also, the abstract of the disclosure was objected to in the first Office Action because it did not contain key terms of the invention, and it contained the word "preferably". The abstract has been amended to include key terms as suggested, e.g. instruction window buffer, multi-processor, and parallel processing environments, to remove the word preferably, and to remove purported merits of the invention. An amended abstract is also included in the Amendments to the Specification.

In the Office Action dated October 22, 2003, applicants were required under 37 C.F.R. 1.105 to provide the title, citation, and copy of each publication that was a source used for the description of the prior art in the disclosure. Please find enclosed the following documents submitted in satisfaction of this requirement: Invention Disclosure Citation, Statement of Relevance, and copies of the six cited references. In addition, the requisite fee under 37 C.F.R. 1.17(p) is submitted for filing an Invention Disclosure Citation under 37 C.F.R. 1.97(c).

Applicants note that the Office Action Summary sheet indicated that claims 1-14 were subject to restriction and/or election requirement. However, there was no mention of such a requirement in the Detailed Action. Applicants understand that claims 1-14 were rejected in the Detailed Action rather than subject to a restriction or election requirement and believe that the restriction/election box was marked in error. However, if any claims are subject to a restriction or election requirement, applicants respectfully request clarification so that they may have an opportunity to respond appropriately.

In the Office Action dated October 22, 2003, claim 6 was rejected under 35 U.S.C. 112, first paragraph as failing to comply with the enablement requirement because of undue breadth. Applicants respectfully traverse this rejection for the reasons below.

First, applicants respectfully submit that applicants do describe in the specification how to make and use the invention, as claimed in currently amended claim 6. For example, Paragraph 28 and FIG. 1 describe one embodiment of a "buffer storage device having a plurality of entries" as buffer 10 memory that has a plurality of 64 entries. Applicants maintain that one of ordinary skill in the art would readily recognize that a memory is a storage device. Paragraphs 45 and 62 provide support for "the entries being subject to processing by at least one process." One embodiment of "means for generating an active bit string for each of said at least one process, wherein the active bit string comprises status information for the entries" is described in Paragraphs 46 through 50 with reference to FIG. 3. "[T]he status information of an entry of said entries indicates readiness of the entry for further processing by said at least one process" is described for the exemplary processes of dispatch, commit, and purge in Paragraphs 52 through 56 and Paragraph 59. Therefore, applicants respectfully submit that the scope of claim 6 is commensurate with the description provided in the specification. Consequently, Applicants respectfully request that the rejection of claim 6 under 35 U.S.C. 112, first paragraph be withdrawn in light of current amendments to claim 6 and for the reasons stated above.

In the Office Action dated October 22, 2003, claims 6-8 and 9-11 were rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Applicants respectfully traverse this rejection for the reasons below. Applicants understand the Examiner's ground for rejecting claims 6-8 to be that original claims 6-8 recite a single means that does not appear in combination with another recited element of means. Applicants respectfully submit that the current amendments to claims 6-8 overcome this ground for rejection because claim 6, as currently amended, recite two means - means for generating an active bit string for each of said at least one process and means for computing the status information. Moreover, the following recitation in claim 6 explains how the two elements relate to one another: "wherein the active bit

string comprises status information for the entries, and wherein the status information of an entry of said entries indicates readiness of the entry for further processing by said at least one process."

Applicants respectfully submit that the current amendment of claim 6 also overcomes the rejection of claims 7, 8, 10, and 11 for the reasons stated above because claims 7, 8, 10, and 11, as currently amended, depend from claim 6. Claim 9 has been canceled as indicated above in Amendment to the Claims. In addition, with respect to claims 10 and 11, applicants respectfully submit that the further recitation in each of these claims, which makes reference to a preceding claim to define a limitation, is in compliance with MPEP §2173.05(f). With respect to claim 10, applicants also respectfully traverse the rejection of claim 10 as currently amended under 35 U.S.C. 112, second paragraph on the ground of insufficient antecedent basis for "sub-unit". The term sub-unit has been deleted by amendment in favor of "buffer storage device," which has support in the claim and the specification. Therefore, applicants respectfully request that the rejection of claims 6-8, 10, and 11 under 35 U.S.C. 112, second paragraph be withdrawn.

Substantively, claims 1-3, 5-8, and 12-14 were rejected under 35 U.S.C. 102(b) as being unpatentable over Soell et al. (U.S. Patent No. 5,923,900; hereinafter, Soell). Applicants respectfully traverse this rejection for the reasons below. The present invention and Soell address different problems: the present invention relates to a method and system for determining the status, i.e. readiness for further processing, of entries in an instruction window buffer of a parallel processing environment; in contrast, the Soell reference is directed to determining the sequential priority of active entries in an instruction window buffer. More particularly, Soell describes an "active bit string" (206) which consists of 64 bits corresponding to the 64 circular buffer entries" where [t]he sequence of 1's in said active bit string (206) thus indicates the sequence of entries in the circular buffer ranging from the out-pointer (201) to the entry position preceding the in-pointer (203)." Soell then describes the active bit string as an input to a circuit that determines the sequential priority of instructions stored in an instruction window buffer. (FIG. 7; col. 6, lines 12-31.)

That is, Soell *defines* what the active bit string is and describes *using* an active bit string to identify the status of entries in a circular instruction window buffer, but does not teach or suggest the claimed method of operating a buffer memory in accordance with aspects of the

present invention recited in claim 1 as currently amended. For example, Soell does not teach or suggest generating an active bit string comprising the status information of buffer entries wherein the computing of the status information of an entry includes the following:

(i) comparing an entry index of the entry to an out-pointer to determine whether the entry index is greater than or equal to the out-pointer; (ii) comparing the entry index of the entry to an in-pointer to determine whether the entry index is less than the in-pointer; [and] (iii) determining whether a buffer wrap around has occurred, and one of the comparing (i) and the comparing (ii) is true, and if so, setting the status information of the entry to a value which indicates readiness of the entry for further processing by the at least one process.

Soell suggests that the active bit string (206) (FIG. 2B) is derived only from an in-pointer (201) and out-pointer (203) (see, e.g., FIG. 2B). Soell does not teach or suggest utilizing wrap around signal (211) to generate active bit string (206).

Moreover, FIG. 2B of Soell teaches away from applicants claimed invention because FIG. 2B shows elements of active bit string (206) and wrap around signal (211) as inputs to unfold circuits (208) and (209), which generate an extended active bit string (214). In Soell, extended bit string (214) is *derived from* active bit string (206). Additionally, the extended active bit string (214) in Soell functions as part of a technique for determining the sequential priority of processing entries in a circular buffer that are ready for processing in a computing environment in which the number of entries ready for processing exceeds the number of available processors. Since the extended active bit string in Soell is used to address a different problem related to out-of-order processing than the present invention, applicants respectfully submit that the extended active bit string in Soell is not equivalent to the claimed active bit string, and, therefore Soell does not teach or suggest computing of the status information of an entry comprising “determining whether a buffer wrap around has occurred.”

Assuming *arguendo* that Soell extended active bit string is viewed as functionally equivalent to the claimed active bit string, applicants respectfully submit that their invention claimed is patentably distinct from the teachings and suggestions of Soell. For example, Soell’s unfold circuit (400), consisting of field-effect transistors (404) and (406) and inverter (403), generates elements two elements of the extended active bit string (405) and (407), but Soell does

not teach or suggest "determining whether ... one of the comparing (i) and the comparing (ii) is true". (Soell, FIG. 4 and col. 4, lines 35-47.) The switching of an input to one of two outputs taught by Soell does not teach or suggest the claimed "determining whether ... one of the comparing (i) and the comparing (ii) is true."

Because Soell does not teach or suggest all aspects of the present invention recited in claims 1, 6, and 12 as currently amended, applicants respectfully submit that these claims recite patentable subject matter over the applied reference. Applicants thus respectfully request withdrawal of the rejection of claims 1, 6, and 12, as currently amended, based on Soell. In addition applicants, respectfully request withdrawal of the rejection of claims 2, 3, 5, 7, 8, 13 and 14, as currently amended, for the reasons stated above for claims 1, 6, and 12, as currently amended, and for their own additional recitations because these claims depend from claims 1, 6, and 12, as currently amended.

In the Office Action dated October 22, 2003, claims 4 and 9-11 were rejected under 35 U.S.C. 103(a) as being unpatentable over Soell in view of Hilgendorf et al. (U.S. Patent No. 5,930, 491; hereinafter, Hilgendorf). Applicants respectfully traverse this rejection for the reasons stated below. Claim 9 has been canceled as indicated above in Amendment to the Claims. As discussed above with respect to the patentability of claims 1, 6, and 12, as currently amended, Soell does not teach or suggest generating an active bit string comprising the status information of buffer entries wherein the computing of the status information of an entry includes the following:

(i) comparing an entry index of the entry to an out-pointer to determine whether the entry index is greater than or equal to the out-pointer; (ii) comparing the entry index of the entry to an in-pointer to determine whether the entry index is less than the in-pointer; [and] (iii) determining whether a buffer wrap around has occurred, and one of the comparing (i) and the comparing (ii) is true, and if so, setting the status information of the entry to a value which indicates readiness of the entry for further processing by the at least one process.

Hilgendorf does not overcome this deficiency because it does not describe generating an active bit string comprising the status information of buffer entries. In contrast, Hilgendorf describes a method of generating a sequence of instruction identification numbers for internal instructions so

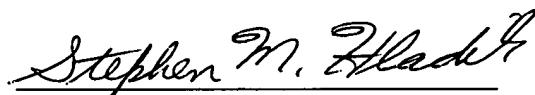
that a sequence of internal instructions in a window buffer can be identified as related to an external instruction easily in an out-of-order processor environment (col. 2, line 61 to col. 3, line 17).

Applicants respectfully request withdrawal of the rejection of claims 4 and 10, as currently amended, and 11 and allowance thereof for the reasons stated above with respect to claims 1 and 6, as currently amended, and for their own additional recitations.

For the reasons discussed hereinabove, applicants respectfully request allowance of all pending claims, namely claims 1-8, 10-14, and 15-17, as currently amended and as currently added by amendment.

Should the Examiner wish to discuss this case with applicants' attorney, please contact applicants' attorney at the below listed number.

Respectfully submitted,



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Dated: February 23, 2004.

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